LINXIAO WU

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EDUCATION

Columbia University New York, NY
M.S. in Electrical Engineering, GPA: 4.082/4.0 Expected Dec 2026
Courses: VLSI Design Lab, Digital VLSI Circuits, Advanced Logic Design, Computer Hardware Design, Formal Verification

Sun Yat-Sen University Guangzhou, CN
B.Eng. in Microelectronic Science and Engineering, GPA: 3.7/4.0 Jun 2025
Course: Analog Circuits Design, Embedded System, FPGA Design, Digital Signal Processing.
Honor: Recipient of the Sun Yat-sen University Scholarship; Outstanding Undergraduate Thesis Award.

EXPERIENCE

Guangzhou CanSemi Technology Inc. Guangzhou, CN
Intern Jul 2024 - Sep 2024

- Calibrated a 32 V PMOS TCAD model to foundry recipe data, and delivered a reusable device model.
- Performed wafer electrical characterization and data analysis to support wafer acceptance testing (WAT), collaborating with process and test teams to improve inspection accuracy and consistency.
- Simulated electrical characteristics of two insulated-gate bipolar transistor (IGBT) structures and contributed as a co-inventor in a patent application for a novel device design.

PROJECTS

Apple-Sponsored Student Tape-Out Project Feb 2026 - Present
A Systolic Array-based CNN Accelerator for Gesture Recognition

- Designed a pure-hardware INT8 CNN accelerator ASIC for 64×64 grayscale gesture recognition with a fixed CNN architecture.
- Architected and implemented a 64-PE INT8 systolic-array accelerator supporting ~464k MACs per inference and ~16 KB on-chip SRAM in 65nm.
- Completed the full digital IC design flow, including RTL implementation, synthesis with Cadence Genus, place-and-route with Innovus, timing closure, and post-layout verification.
- Built and quantized CNN models in Python and MATLAB, and optimized network structure to balance accuracy, area, and hardware cost.

Out-of-Order RISC-V Processor Mar 2026 - Present
Project, Columbia University,

- Designed a P6-style out-of-order RISC-V microarchitecture featuring key structures including a reorder buffer (ROB), register alias table (RAT), reservation stations, and a physical register file (PRF).
- Implemented register renaming and physical register allocation with a free-list mechanism to eliminate WAR/WAW hazards and improve instruction-level parallelism (ILP).
- Built precise commit and exception recovery mechanisms based on the ROB to support speculative execution.
- Designed a reservation-station scheduling and Common Data Bus (CDB) forwarding mechanism to enable out-of-order issue and execution.

64-tap 16-bit FIR Digital Filter Core Oct 2025 - Dec 2025
Project, Columbia University

- Designed a fixed-point 64-tap 16-bit FIR filter core, including a multiply-accumulate datapath, CMEM/IMEM, and an FSM-based controller.
- Adopted a single-MAC plus FSM reuse architecture to balance hardware area and performance.
- Implemented a dual-clock FIFO to handle clock-domain crossing (CDC) between the 10 kHz input clock domain and the high-speed FIR core
- Completed RTL implementation, logic synthesis in Design Compiler, static timing analysis (STA) in PrimeTime, and post-synthesis functional verification.

8-bit Microcontroller Core Design Oct 2025 - Dec 2025
Project, Columbia University

- Designed an 8-bit accumulator-based microcontroller at the transistor level in TSMC 65 nm using a custom 6-bit ISA
- Implemented key modules including PLA-based control logic, multiplexers, shift bypasser, accumulator, memory latch, bus driver, 8-bit adder, shifter, and 8-byte SRAM.
- Completed layout implementation with clean DRC/LVS, and verified ADD, SHIFT, and full-processor functionality through pre-layout and post-layout simulations.
- Performed post-layout performance analysis, achieving a 354 ps critical path and a core area of approximately 7,267.49 μm^2.

TECHNICAL SKILLS

Simulation & EDA Tools: Cadence (Virtuoso, Spectre, Genus, Innovus), Synopsys (PrimeTime), Vivado, Questa Sim, JasperGold
Programming: Verilog, SystemVerilog, RISC-V, Python(Numpy, PyTorch), C, MATLAB
Design Expertise: ASIC Design Flow, Digital Circuit Design, CNN Accelerators, SAR ADC, Digital Calibration